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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/639,753	08/15/2000	Takehiro Ohkawa	NIT-217	4173

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EXAMINER	
YANG, CLARA I	
ART UNIT	PAPER NUMBER
2635	2

DATE MAILED: 03/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/639,753	Applicant(s) OHKAWA ET AL.	
	Examiner Clara Yang	Art Unit 2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *02* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 7 March 2000. It is noted, however, that applicant has not filed a certified copy of the 2000-067141 application as required by 35 U.S.C. 119(b).

Information Disclosure Statement

2. The information disclosure statement filed on 15 August 2000 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 - 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Carroll U.S. Patent No. 4,857,893.

Referring to Claim 1, Carroll's single chip transponder device 14 or radio frequency identification device (RFID) comprises: (a) an antenna 20, as shown in Figs. 1, 5, and 9A - 9B, for receiving power to enable a semiconductor circuit device (hereinafter referred to as "transponder 14") to transmit and receive signals (see Col. 3, lines 37 - 41 and Col. 6, lines 13 -

18 and 38 - 43); and (b) rectifier/balanced modulator circuit 22 (see Fig. 5) or first means for powering transponder 14 (i.e., releasing transponder 14 from its reset state) upon detection of a condition that a voltage attained by rectifying an alternating current (AC) wave induced on antenna 20 is higher than a predetermined voltage level (see Col. 6, lines 38 - 43; Col. 7, lines 67 - 68; and Col. 8, lines 1 - 31). Once the requisite supply voltage, such as 6 volts, is maintained, Carroll discloses that transponder 14 generates an encoded data word that is mixed with the modified carrier signal by rectifier/balanced modulator circuit 22 and transmits the resulting signals via antenna 20 (see Col. 6, lines 22 - 37). Per the teachings of Carroll, rectifier/balanced modulator circuit 22 comprises a diode bridge formed by diodes 60, 61, 62, and 63. A Zener diode 66 is incorporated into the bridge circuit in order to stabilize the voltage VDD that is generated (see Col. 7, lines 67 - 68 and Col. 8, line 1). Because the bridge circuit uses the capacitance inherent in all the circuit elements present on the chip to help store the energy needed to maintain a sufficiently constant supply voltage VDD, it is implied that the bridge circuit controls the impedance state of transponder 14 (see Col. 8, lines 1 - 6). Furthermore, Carroll imparts that when complementary metal oxide semiconductor (CMOS) circuits are used, supply voltage VDD must be maintained at a prescribed level, such as 6 volts, in order for the CMOS circuits to transmit data (see Col. 8, lines 12 - 17), thus implying that transponder 14's data transmission is controlled by its state of impedance (i.e., the state of impedance must be high in order for transponder 14 to transmit). Because Zener diode 66 functions as a normal rectifier until the voltage applied to it exceeds a threshold voltage, which then causes the diode to become conducting, it is inherent that Zener diode 66 turns off and places transponder 14 in a reset state or a low impedance state when the applied DC voltage is lower than Zener diode 66's threshold or avalanche voltage.

Regarding Claims 2 and 3, it is understood that Zener diode 66's threshold or avalanche voltage is both the reset release voltage (i.e., when Zener diode 66 becomes conducting) and the reset voltage (i.e., when Zener diode 66 returns to functioning as a normal rectifier). Because Carroll suggests a supply voltage VDD of 6 volts in order for transponder 14's semiconductor device or integrated circuit (IC) to operate, supply voltage VDD is understood to be the IC's logic working guarantee voltage. In order for Zener diode 66 to provide a stable supply voltage VDD, the voltage applied to Zener diode 66 must reach a certain threshold value in order for the diode to become conducting, thus implying that the reset release voltage must be substantially equal to the IC's logic working guarantee voltage of, for example, 6 volts.

Referring to Claim 4, Carroll's transponder 14 or RFID comprises: (a) an antenna 20 (see Figs. 1, 5, and 9A - 9B); and (b) rectifier/balanced modulator circuit 22 (see Figs. 4 and 5) or first means that has a Zener diode 66 for releasing a reset state of transponder 14 upon detection of a condition that a DC voltage attained by rectifying an AC wave induced on antenna 20 is higher than a threshold level as explained above in Claims 2 and 3 (see Col. 6, lines 38 - 43; Col. 7, lines 67 - 68; and Col. 8, lines 1 - 31). Because rectifier/balanced modulator circuit 22's bridge circuit (see Fig. 5, diodes 60, 61, 62, and 63) uses the capacitance inherent in all the circuit elements present on the chip to help store the energy needed to maintain a sufficiently constant supply voltage VDD (see Col. 8, lines 1 - 6), it is implied that the bridge circuit controls the impedance state of transponder 14 (i.e., transponder 14 has a high state of impedance when supply voltage VDD is provided). Carroll discloses that transponder 14 generates an encoded data word that is mixed with the modified carrier signal by rectifier/balanced modulator circuit 22 and transmits the resulting signals via antenna 20 (see Col. 6, lines 22 - 37). Carroll further imparts that a Zener diode 66 is incorporated into the bridge circuit in order to stabilize the voltage VDD that

is generated (see Col. 7, lines 67 - 68 and Col. 8, line 1). Because a Zener diode functions as a normal rectifier until the voltage applied to it exceeds a threshold voltage, which then causes the diode to become conducting, it is inherent that when the applied DC voltage is lower than Zener diode 66's threshold or avalanche voltage, Zener diode 66 returns to functioning as a normal rectifier and no longer provides the required supply voltage VDD thus placing transponder 14 in a reset state or a low impedance state.

Referring to Claims 5 - 8, Carroll's transponder 14, as shown in Fig. 9A, comprises: (a) an IC element having a programmable memory array 102, a logic circuit 100, and rectifier/balanced modulator circuit 22 (see Figs. 4 and 5) or power-on-reset means (see Col. 11, lines 11 - 27); and (b) an antenna 20 for receiving power and signals from an external apparatus and for supplying power and signals to transponder 14's memory 102, which comprises memory array 80 in Fig. 4, and data generator 30 of logic circuit 100 (see Fig. 1, controller/interrogator 12 and interrogation signal 16; Col. 3, lines 37 - 41 and Col. 6, lines 13 - 18 and 22 - 43). Carroll also imparts that a Zener diode 66 is incorporated into rectifier/balanced modulator circuit 22 in order to stabilize the voltage VDD that is generated (see Col. 7, lines 67 - 68 and Col. 8, line 1). Because a Zener diode functions as a normal rectifier until the voltage applied to it exceeds a threshold voltage, which then causes the diode to become conducting, it is inherent that Zener diode 66 returns to functioning as a normal rectifier when the applied DC voltage is lower than Zener diode 66's threshold voltage and no longer provides the required supply voltage VDD, thus placing transponder 14 in a reset state or a low impedance state. In addition, Carroll imparts that: (c) IC element comprises communication means (see Col. 6, lines 12 - 37), and (d) rectifier/balanced modulator circuit 22's bridge circuit (see Fig. 5, diodes 60, 61, 62, and 63) uses the capacitance inherent in all the

circuit elements present on the chip to help store the energy needed to maintain a sufficiently constant supply voltage VDD (see Col. 8, lines 1 - 6), thus implying that the bridge circuit controls the impedance state of transponder 14 (i.e., transponder 14 has a high state of impedance when supply voltage VDD is provided). Carroll further discloses that when a supply voltage VDD is maintained at a prescribed level, transponder 14 generates an encoded data word that is mixed with the modified carrier signal by rectifier/balanced modulator circuit 22 and transmits the resulting signals via antenna 20 (see Col. 6, lines 22 - 37).

5. Claims 1, 4, 6, 8, 9, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Beigel U.S. Patent No. 4,333,072.

Referring to Claims 1, 4, 6, 8, and 9, because Beigel's tag circuit 67 or RFID is a very small identification device (see Col. 4, lines 29 - 31), it is understood that tag circuit 67, as shown in Fig. 2, is an IC element. Still referring to Fig. 2, tag circuit 67 comprises: (a) CMOS 8-channel multiplexer circuit 83 or communication means, CMOS counter 81 or a logic circuit, and capacitor 71, diode 73, and Zener diode 77 that form a first means for releasing a reset state or power-on-reset means (see Col. 6, lines 17 - 67); and (b) a coil 65 or antenna for receiving power and signals from a probe or external apparatus and for supplying the power and signals to the communication means and counter 81 (see Col. 4, lines 1 - 4 and 31 - 37; and Col. 6, lines 2 - 10 and 17 - 25). Since a Zener diode functions as a normal rectifier until the voltage applied to it exceeds a threshold voltage, which then causes the diode to become conducting, it is inherent that when the applied DC voltage is lower than Zener diode 77's threshold or avalanche voltage, Zener diode 77 returns to functioning as a normal rectifier and no longer provides the required supply voltage VDD, thus placing Beigel's tag circuit 67 in a reset state or a low impedance state. Beigel further discloses that when the voltage developed across tag coil 65 is

sufficient to power tag circuit 67, counter 81 sends control signals to multiplexer circuit 83, wherein each of the eight switching devices in circuit 83 (see Fig. 2, pins 0 - 7 on CD4051) causes the load on coil 65 to vary in accordance with counter 81's counting sequence (see Col. 6, lines 6 - 9 and 48 - 67). Beigel teaches that one terminal of each switching device is connected to coil 65 and that the other terminal of each switching device is connected to coil 65 via resistor 87 (see Col. 6, lines 55 - 62). Here it is understood that resistor 87 is a load resistor. According to Beigel, a unique code is created for tag circuit 67 by either conductively coupling or insulating terminals in a particular pattern. When terminal pairs of each switch are mutually conductively coupled (see Channels 0, 3, 5, and 6 of CD4051 in Fig. 2), they will load the circuit of the inductor coil 65 (i.e., more current is drawn by coil 65). However, when the terminal pairs of each switch are insulated (see Channels 1, 2, 4, and 7 of CD4051 in Fig. 2), they will not load the circuit of the inductor coil 65 (i.e., less current is drawn by coil 65). (See Col. 7, lines 3 - 44). Consequently, it is understood that multiplexer 83 is a switching element that either connects (via switches with coupled terminals) or disconnects (via switches with insulated terminals) load resistor 87 from a ground potential within multiplexer 83. The varying load on coil 65 is reflected in the voltage across the external apparatus' coil 61, and the external apparatus is able to ascertain tag circuit 67's unique code by measuring the power consumption (see Col. 6, lines 10 - 16).

Referring to Claim 10, as shown in Fig. 2, Beigel's tag circuit 67 comprises: (a) CMOS 8-channel multiplexer circuit 83 or communication means, CMOS counter 81 or a logic circuit, and capacitor 71, diode 73, and Zener diode 77 that form a power-on-reset means (see Col. 6, lines 17 - 67); and (b) a coil 65 or antenna for receiving power and signals from a probe or external apparatus and for supplying the power and signals to the communication means and counter 81

(see Col. 4, lines 1 - 4 and 31 - 37; and Col. 6, lines 2 - 10 and 17 - 25). As shown in Fig. 2, one terminal of load resistor 87 is connected to coil 65 whereas the other terminal of load resistor 87 is connected to multiplexer 83 (i.e., a switching element). When the voltage applied to the power-on-reset means is lower than the threshold voltage of Zener diode 77, counter 81 and multiplexer 83 are inactive. Consequently, load resistor 87 is connected to a ground potential through multiplexer 83.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Bickley et al. U.S. Patent No. 5,430,441: Bickley's passive RFID comprises an antenna for receiving power and signals from an external device, a rectifying circuit for supply power the semiconductor device, a voltage threshold sensor for switching the RFID between an active or inactive state based on the sensed voltage level, and a modulator for varying the impedance of the antenna in accordance to its response code.

- Turner et al. U.S. Patent No. 5,793,305: Turner's passive RFID comprises an antenna for receiving power and signals from an external device, a rectifying circuit for supply power the semiconductor device, and a modulator for varying the impedance of the antenna in accordance to its response code.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clara Yang whose telephone number is (703) 305-4086. The examiner can normally be reached on 8:30 AM - 7:00 PM, Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Horabik can be reached on (703) 305-4704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

CY
February 24, 2003

BRIAN ZIMMERMAN
PRIMARY EXAMINER